PROCESS FOR MAKING LARGE AREA ISOLATION TRENCHES UTILIZING A TWO-STEP SELECTIVE ETCHING TECHNIQUE

FIELD OF THE INVENTION

The method generally relates to methods for making wide, deep trenches in semiconductor material and for filling such trenches with dielectric material for providing low capacitive substrate regions for supporting signal carrying surface conductors.

DESCRIPTION OF THE PRIOR ART

Large scale integrated circuit fabrication requires that signal carrying surface conductors be provided to connect the individual active and passive circuit elements into functional configurations. It is desirable, of course, that such surface conductors be isolated effectively from the semiconductor substrate so that unwanted capacitive coupling to the substrate is minimized.

One technique to minimize unwanted coupling to the substrate is described in U.S. Pat. No. 4,139,442, issued to Bondur et al. on Feb. 13, 1979, for "Reactive Ion Etching Method For Producing Deep Dielectric Isolation in Silicon", in the names of James Bondur et al. and assigned to the present assignee. Briefly, the technique provides a narrow-line width oxide masking layer for the reactive ion etching of multiple deep trenches in a silicon substrate. The deep trenches are separated from each other by thin walls of silicon determined by the oxide mask line width. The silicon walls are later fully converted to silicon oxide by a thermal oxidation step.

It is important that the thickness of the walls of silicon be closely controlled so that they are thick enough for structural strength to prevent breaking and yet not too thick for reasonable thermal oxidation times. Even with the use of electron beam photoresist technology, to delineate the oxide mask line width, it is difficult to achieve the required degree of control when writing narrow line widths of about 0.5 micrometers.

SUMMARY OF THE INVENTION

A precisely controllable, narrow line width masking layer for etching semiconductor substrates is formed by a process which includes the step of selectively etching a semiconductor substrate to produce a spaced succession of narrow, shallow trenches having substantially vertical walls. A conformal coating of a masking material is deposited on the etched substrate and the coated substrate is etched so as to remove the conformal coating from the horizontal surfaces of the etched substrate while leaving the coating on the vertical surfaces of the etched substrate.

With the remaining masking material in place, the substrate is reactively ion etched to produce a spaced succession of narrow, deep trenches separated by narrow semiconductor mesas, the alternate trenches being of equal first depth and the intervening alternate trenches being of equal second depth different from the first depth. The width of each of the silicon mesas is substantially equal to and determined by the thickness of the deposited conformal coating. Thus, the width of the mesas is controlled to the same high degree as is the thickness of the coating.

The resulting structure is thermally oxidized sufficiently to completely oxidize the semiconductor material underneath the remaining deposited conformal coating and the remaining trench volume is filled with dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**, **2**, **3**, **4** and **5** are simplified cross-sectional views of the structure obtaining at successive times during the fabrication of a wide, deep recessed oxide isolation trench in a silicon semiconductor substrate in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The structure of FIG. **1** includes monocrystalline silicon substrate **10** which is shown as P^- conductivity type for illustration purposes, N^+ layer **12** over the substrate **10** and N^- conductivity layer **14** on the layer **12**. For the purposes of the invention, either all or some of the layers **10**, **12** and **14** could be of opposite conductivity type from the conductivity types indicated. However, it is preferred that layer **12** be of high conductivity where localized portions of it later become the subcollectors of bipolar transistors.

The structure of FIG. **1** can be fabricated by various techniques. The preferred technique, however, is to provide a P^- monocrystalline silicon substrate **10** and to diffuse an N^+ blanket diffusion into the substrate (to produce region **12**) by using conventional diffusion or ion implantation of an N-type impurity such as arsenic, antimony or phosphorous to produce an N^+ region with a surface concentration of between about 1×10^{19} to 1×10^{21} atoms/cc. The layer **14** is subsequently grown over layer **12** by means of epitaxial growth. This may be done by conventional techniques, such as by the use of $SiCl_4/H_2$ or SiH_4/H_2 mixtures at growth temperatures of about 1,000° C. to 1,200° C. The N^+ layer may have a typical thickness of from about 1 to 3 microns whereas the epitaxial layer may have a thickness of from about 0.5 to 10 microns, the exact thicknesses depending upon the device to be built.

Alternatively, the structure could be made by various combinations of thermal diffusion, ion implantation and/or epitaxial growth which would include the formation of a buried subcollector region where subsequent formation of bipolar transistors is desired. In certain device structures, buried highly doped regions or layers are not necessary and can therefore be omitted. This is true for FET type devices. Alternatively, multiple buried highly doped regions of different dopant types could be formed by multiple epitaxial and diffusion processing. These structures could be needed for buried subcollectors as well as for buried conductor lines.

The silicon structure comprising substrate **10**, N^+ layer **12** and N^- layer **14** is patterned by conventional photolithography techniques (not shown) and is selectively etched to produce narrow, shallow trenches **16** having substantially vertical walls **18** and horizontal bottom surfaces **20**, as shown in FIG. **1**. As will be described more fully later, the width of the shallow trenches **20** is of the order of about 2.5 microns or less so that when filled with a combination of thermal oxide and chemical-vapor-deposited oxide (or other chemical-vapor-deposited material), the trenches primarily are filled by deposits built up on the vertical walls, i.e., the trenches are filled in an inward direction by deposits on the sidewalls rather than in an upward direction by deposits on the trench bottoms. This is distinguished